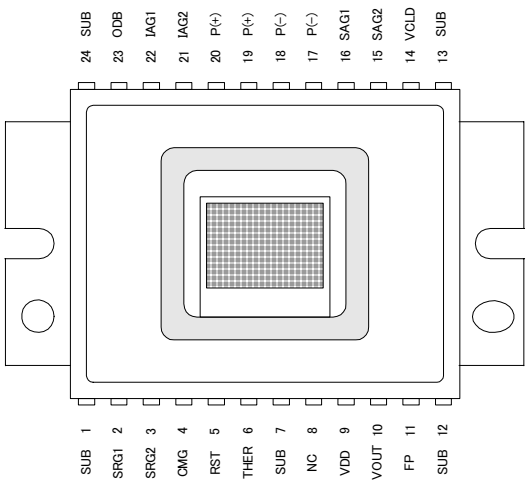
- **Very Low Noise, Very High Sensitivity, Electronically Variable Charge Domain Gain**
- **1/2-in Format, Solid State Charge-Coupled Device (CCD) Frame Interline Transfer Monochrome Image Sensor for Low Light Level Applications with 30 Frames/s readout speed**
- **340,000 Pixels per Field**
- **Frame Memory**
- **658 (H) x 496 (V) Active Pixels in Image Sensing Area**
- **Multimode Readout Capability**
  - **Progressive Scan**
  - **Pseudo-Interlace Scan**
  - **Line Summing**
  - **Pixel Summing**
- **0-8V Serial Operation Except CMG Gate**
- **Continuous Electronic Exposure Control from 1/30 s to 1/2,000 s**
- **Advanced Lateral Overflow Drain**
- **10.0 um Square Pixels**
- **Low Dark Current**

DUAL-IN-LINE PACKAGE (TOP VIEW)



- **High Photoresponse Uniformity Over a Wide Spectral Range**
- **Solid State Reliability With No Image Burn-in, Residual Imaging, Image Distortion, or Microphonics**
- **Package with built-in Peltier Cooler and Temperature Sensor**

Description

The TC247SPD is a frame interline transfer CCD image sensor designed for use in black and white, NTSC TV, computer, and special-purpose applications requiring low noise, high sensitivity, high speed and low smear.

The TC247SPD is a new device of the IMPACTRON™ family of very-low noise, high sensitivity, high speed and low smear sensors that multiply charge directly in the charge domain before conversion to voltage. The charge carrier multiplication (CCM) is achieved by using a low-noise single-carrier, impact ionization process that occurs during repeated carrier transfers through high field regions. Applying multiplication pulses to specially designed gates activates the CCM. Multiplication gain is variable by adjusting the amplitude of the multiplication pulses. The device function resembles the function of an image intensifier implemented in solid state.

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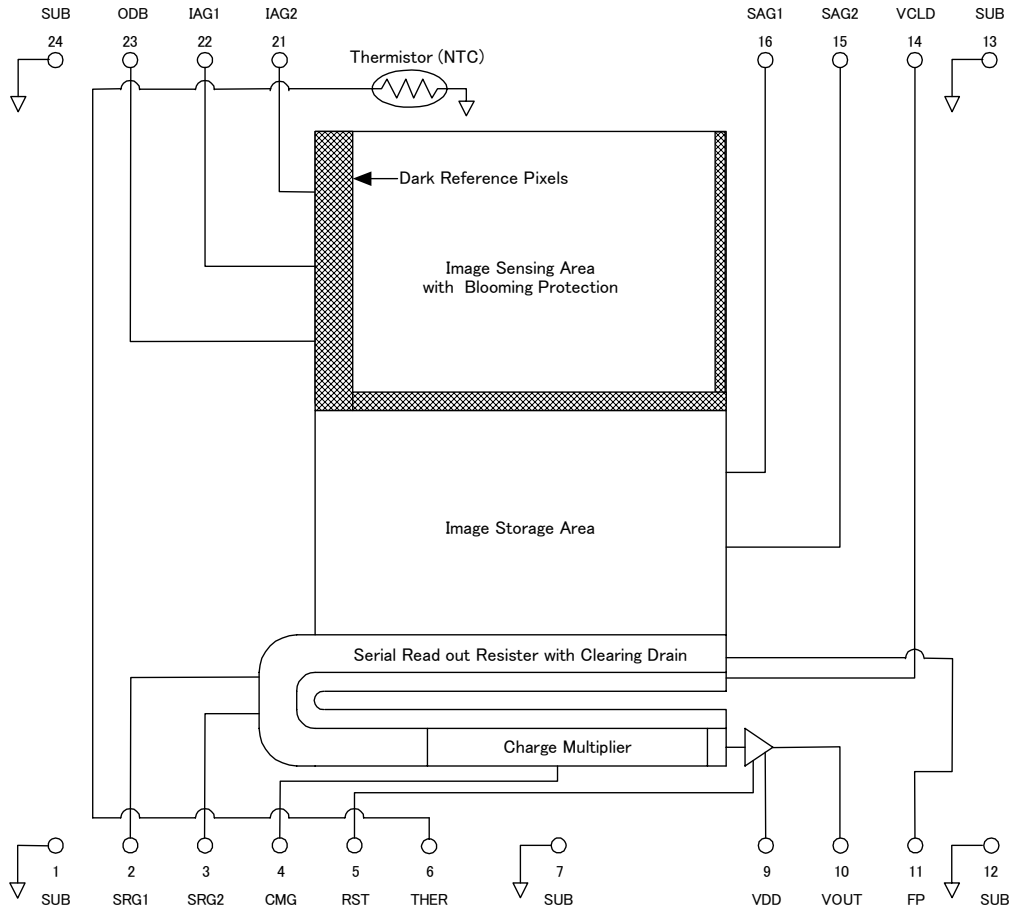
The image-sensing area of the TC247SPD is configured into 500 lines with 680 pixels in each line. 20 pixels are reserved in each line for dark reference. The blooming protection is based on an advanced lateral overflow drain concept that does not reduce NIR response. The sensor can be operated in the progressive scan mode and can capture a full 340,000 pixels in one image field. The frame interline transfer from the image sensing area to the memory area is implemented to minimize image smear. After charge is integrated and stored in the memory it is available for readout in the next cycle. This is accomplished by using a unique serial register design that includes special charge multiplication pixels.

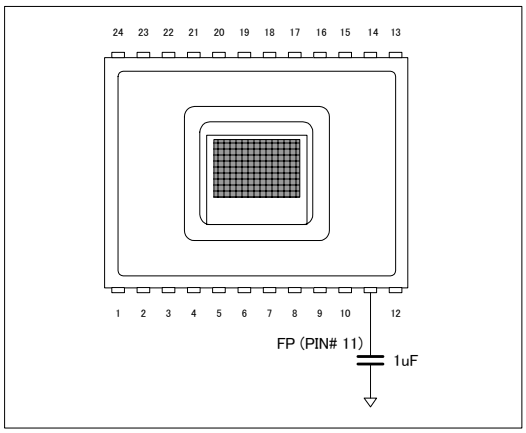
The TC247SPD sensor is built using TI-proprietary advanced Split-Gate Virtual-Phase CCD (SGVPCCD) technology, which provides devices with wide spectral response, high quantum efficiency (QE), low dark current, and high response uniformity.

This MOS device contains limited built-in protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to Vss. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to Vss during operation to prevent damage to the amplifier. The device can also be damaged if the output and ADB terminals are reverse-biased and excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication “Guidelines for Handling Electrostatic-Discharge-Sensitive (ESD) Devices and Assemblies” available from Texas Instruments.

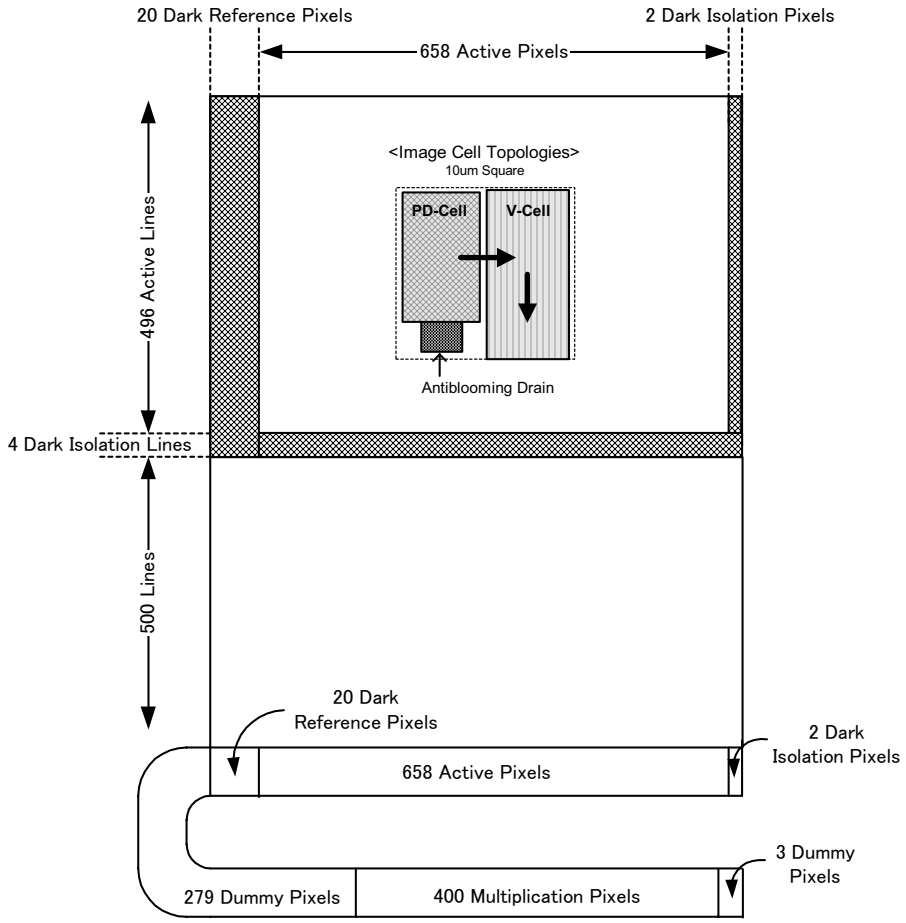
Functional block diagram



For stable operation, a decoupling capacitor (1uF, >5V) needs to be connected externally from the package FP pin to SUB.



Sensor topology diagram



Terminal functions

Terminal name, No.		I/O	Description
SUB	1,7,12,13,24		Chip substrate
SRG1	2	I	Serial register gate-1
SRG2	3	I	Serial register gate-2
CMG	4	I	Charge multiplication gate
RST	5	I	Reset gate
THER	6	I	Thermistor (NTC: Negative Temperature Coefficient)
NC	8	-	No connection
VDD	9	I	Supply voltage for amplifiers
OUT	10	O	Output signal, multiplier channel
FP	11		Field plate (connect external capacitor)
VCLD	14	I	Supply voltage for Clearing drain & ESD protect circuits
SAG2	15	I	Storage area gate-2
SAG1	16	I	Storage area gate-1
P(-)	17,18	I	Peltier cooler power supply - negative
P(+)	19,20	I	Peltier cooler power supply - positive
IAG2	21	I	Image area gate-2
IAG1	22	I	Image area gate-1
ODB	23	I	Supply voltage for anti-blooming drain

Detailed description

The TC247SPD consists of five basic functional blocks: The image-sensing area, the image–storage area, the serial register, the charge multiplier, and the charge detection node with buffer amplifier. The location of each of these blocks is identified in the functional block diagram.

Image-sensing and storage areas

As light enters the silicon in the image-sensing area, electrons are generated and collected in potential wells of the pixels. Applying a suitable DC bias to the antiblooming drain provides blooming protection. The electrons that exceed a specific level, determined by the ODB bias, are drained away from the pixels. After the integration cycle is completed by applying a PD-cell readout pulse to IAG2, charge is transferred from the PD-cell into the V-cell and then quickly transferred into the storage cell where it waits for readout. The lines can be readout from the memory in a sequential order to implement progressive scan, or 2 lines can be summed together to implement a pseudo-interlace scan. 20 columns at the left edge and 2 columns at the right edge of the image-sensing area are shielded from the incident light. These pixels provide the dark reference used in subsequent video-processing circuits to restore the video-black level.

Additionally, 4 dark lines, located between the image sensing area and the image-storage area, were added to the array for isolation.

Advanced lateral overflow drain

Each pixel is constructed with the advanced lateral overflow drain structure. By varying the DC bias of the anti-blooming drain it is possible to control the blooming protection level and trade it for well capacity.

Electronic exposure control

Precise exposure control timing on a frame-by-frame basis is possible. The integration time can be arbitrarily shortened from its nominal length by clearing residual charge from the PD-cell. To do this, apply a PD-cell clear pulse to IAG2, which marks the beginning of integration.

Serial register and charge multiplier

The serial register of TC247SPD image sensor consists of only poly-silicon gates. It operates at high speed, being clocked from 0V to 8V. This allows the sensor to work at 30 frames/s. The serial register is used for transporting charge stored in the pixels of the memory lines to the output amplifier. The TC247SPD device has a serial register with twice the standard length. The first half has a conventional design that interfaces with the memory as it would in any other CCD sensor. The second half, however, is unique and includes 400 charge multiplication stages with a number of dummy pixels that are needed to transport charge between the active register blocks and the output amplifier. Charge is multiplied as it progresses from stage to stage in the multiplier toward the charge detection node. The charge multiplication level depends on the amplitude of the multiplication pulses (approximately 15V~22V) applied to the multiplication gate. Due to the double length of the register, first 2 lines in each field or frame scan do not contain valid data and should be discarded.

Charge detection node and buffer amplifier

The last element of the charge detection and readout chain is the charge detection node with the buffer amplifier. The charge detection node is using a standard Floating Diffusion (FD) concept followed by an on-chip, dual-stage, source-follower buffer. Applying a pulse to the RST pin resets the detection node. Pixel charge summing function can be easily implemented by skipping the RST pulses. To achieve the ultimate sensor performance it is necessary to eliminate kTC noise. This is typically accomplished by using CDS (correlated double sampling) processing techniques. IMPACTRON™ devices have the potential for detecting single electrons (photons) when cooled sufficiently.

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage range, Vss: VDD, VCLD (see Note1)	0V to 15V
Supply voltage range, Vss: ODB	0V to 22V
Input voltage range, Vi: IAG1, SAG1, SAG2	-10V to 10V
Input voltage range, Vi: IAG2	-10V to 13V
Input voltage range, Vi: SRG1, SRG2, RST	0V to 10V
Input voltage range, Vi: CMG	-5V to 22V
Supply voltage range, Vcool: P+ (see Note2)	0V to 5.5V
Supply current range, Icool: P+ (see Note2)	0A to 1.4A
Supply current range, Ith: THER	0A to 0.31mA
Operating free-air temperature range, Ta	-20°C to 55°C
Storage temperature range, Tstg	-30°C to 85°C
Dew point inside the package (see Note2)	Less than -20°C

* Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect the device reliability.

Notes:

1. All voltage values are with respect to substrate terminal.
2. The peltier cooler generates heat during cooling process. Heat must be removed through an external heat sink. In order to avoid condensation upon the surface do not cool the CCD to less than -20 degrees C.

Recommended operating conditions

Description			MIN	NOM	MAX	UNIT
Substrate bias, Vss				0.0		V
Supply voltage, Vdd	VDD		13.5	14.0	14.5	
	VCLD		13.5	14.0	14.5	
	ODB*		4.5		6.5	
Input voltage, Vi	IAG1	High	3.0	3.3	3.6	V
		Low	-5.8	-5.5	-5.2	
	IAG2	High	9.5	10.0	10.5	
		Mid	3.0	3.3	3.6	
		Low	-5.8	-5.5	-5.2	
	SAG1	High	3.0	3.3	3.6	
		Low	-5.8	-5.5	-5.2	
	SAG2	High	3.0	3.3	3.6	
		Low	-5.8	-5.5	-5.2	
	SRG1	High	7.5	8.0	8.5	
		Low		0.0		
	SRG2	High	7.5	8.0	8.5	
		Low		0.0		
	CMG**	High	7.0		22.0	
		Low	-3.0	-2.5	-2.0	
	RST	High	5.5	6.0	6.5	
		Low		0.0		
Clock Frequency, fck	SAG1, SAG2			1.5		MHz
	IAG1, IAG2			1.5		
	SRG1, SRG2, RST			12.5	25.0	
	CMG			12.5	25.0	
Load capacitance	OUT				6.0	PF
Dew point inside the package ***					-20	°C
Operating free-air temperature			-20	25	55	°C

* Adjustment within the specified MIN – MAX range is required to optimize performance.
** Charge multiplication gain depends on high level of the CMG and temperature.
*** -20 degrees should be the minimum temperature of the cooled CCD.

Electrical characteristics over recommended operating ranges of supply voltage at operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Charge multiplication gain *		1	200	2000	-
Excess noise factor for typical CCM gain (Note 3)		1	1.4		-
Dynamic range without CCM gain			63		dB
Dynamic range with typical CCM gain (Note 4)			75		dB
Charge conversion gain without CCM gain (Note 5)			14		uV/e
τ Signal-response delay time (Note 6)			16		ns
Output resistance			320		Ω
Amp. Noise-equivalent signal without CCM gain **			20		e
Amp. Noise-equivalent signal with typ. CCM gain **			1.0		e
Response linearity with no CCM gain			1		-
Response linearity with typ. CCM gain			1		-
Charge-transfer efficiency (Note 7)	Parallel transfer	0.99994		1.0	-
	Serial transfer	0.99994		1.0	-
Supply current			2.0		mA
Ci Input capacitance	IAG1		3		nF
	IAG2		7		
	IAG1-IAG2		3		
	SAG1		4		
	SAG2		5		
	SAG1-SAG2		3		
	SRG1		85		pF
	SRG2		55		
	CMG		25		
	ODB		2,000		
	RST		7		

All typical values are at Ta = 25 °C unless otherwise noted.

* Maximum CCM gain is not guaranteed.

** The values in the table are quoted using CDS = Correlated Double Sampling. CDS is a signal processing technique that improves performance by minimizing undesirable effects of reset noise.

Notes :

3. Excess Noise Factor “F” is defined as the ratio of noise sigma after multiplication divided by M times the noise sigma before multiplication where M is the charge multiplication gain.
4. Dynamic Range is –20 times the logarithm of the noise sigma divided by the saturation–output signal amplitude
5. Charge conversion factor is defined as the ratio of output signal to input number of electrons.
6. Signal-response delay time is the time between the falling edge of the SRG1 pulse and the output-signal valid state.
7. Charge transfer efficiency is one minus the charge loss per transfer in the CCD register. The test is performed in the dark using either electrical or optical input.

Optical characteristics

Ta = 25°C, Integration time = 16.67msec (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Sensitivity with typical CCM gain (Note 8)	No IR-cut filter		3660		V/Lx sec
	With IR-cut filter		620		
Sensitivity without CCM gain (Note 8)	No IR-cut filter		18.3		V/Lx sec
	With IR-cut filter		3.1		
Saturation signal output no CCM gain (Note 9)			400		mV
Saturation signal output Anti blooming Enable no CCM gain(Note 9)			180		
Saturation signal output with typ CCM gain (Note 9)			1500		
Zero input offset output (Note 10)			100		
Blooming overload ratio (Note 11)			500:1		-
Image area well capacity			28k		e
Smear (Note 12)			-84		dB
Dark current (Note 13)			0.01		nA/cm^2
Dark signal (Note 14)			0.01		mV
Spurious non-uniformity	Dark			5.0	mV
	Illuminated	-30		30	%
Column uniformity (Note 15)				2.0	%
Electronic-shutter capability		1/2000		1/30	s

Notes:

8. Light source temperature is 2856 °K. The IR filter used is CM500 1mm thick.
9. Saturation is the condition in which further increase in exposure does not lead to further increases in output signal.
10. Zero input offset is the residual output signal measured from the reset level with no input charge present. This level is not caused by the dark current and remains approximately constant independent of temperature. It may vary with the amplitude of SRG1.
11. Blooming is the condition in which charge induced by light in one element spills over to the neighboring elements.
12. Smear is the measure of error signal introduced into the pixels by transferring them through the illuminated region into the memory. The illuminated region is 1/10 of the image area height. The value in the table is obtained for the integration time of 33.3ms and 1.5 MHz vertical clock transfer frequency.
13. Dark current depends on temperature and approximately doubles every 8 C^o. Dark current is also multiplied by CCM operation. The value given in the table is with the multiplier turned off and it is a calculated value.
14. Dark signal is actual device output measured in dark.
15. Column uniformity is obtain by summing all the lines in the array, finding the maximum of the difference of two neighboring columns anywhere in the array, and dividing the result by the number of lines.

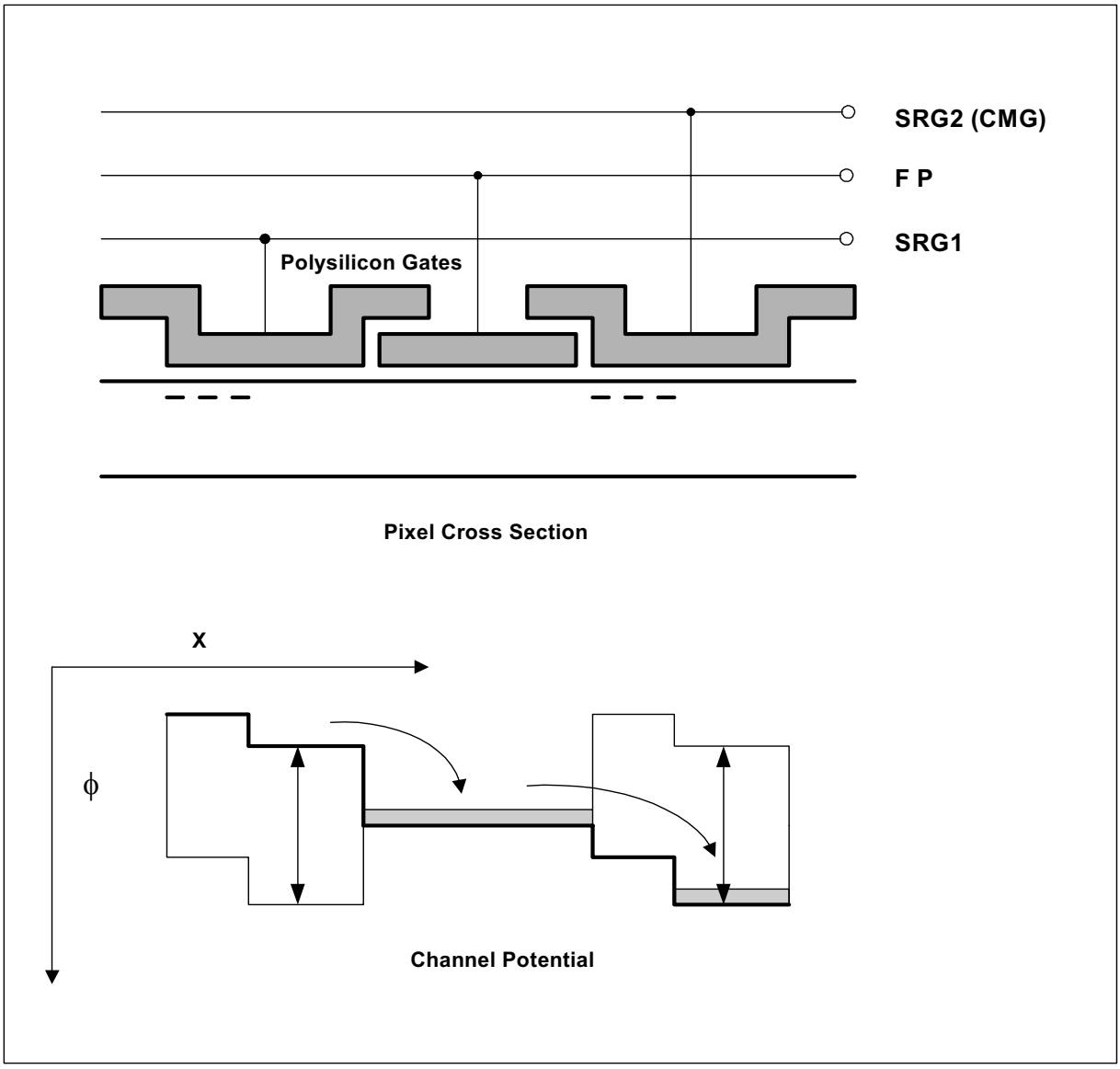


FIGURE 1. Serial Register Pixel Cross Section

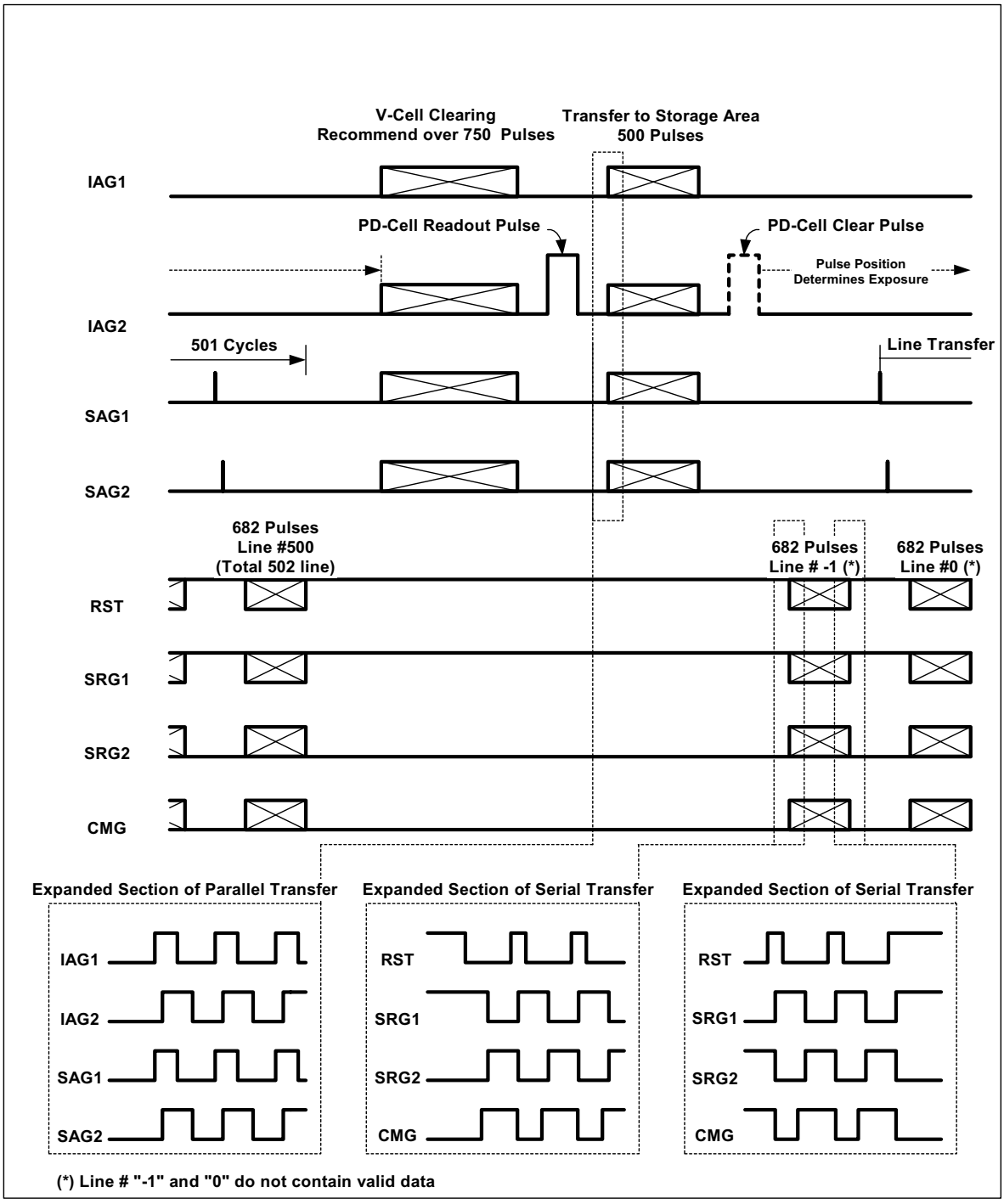


FIGURE 2-a. Progressive Scan Timing

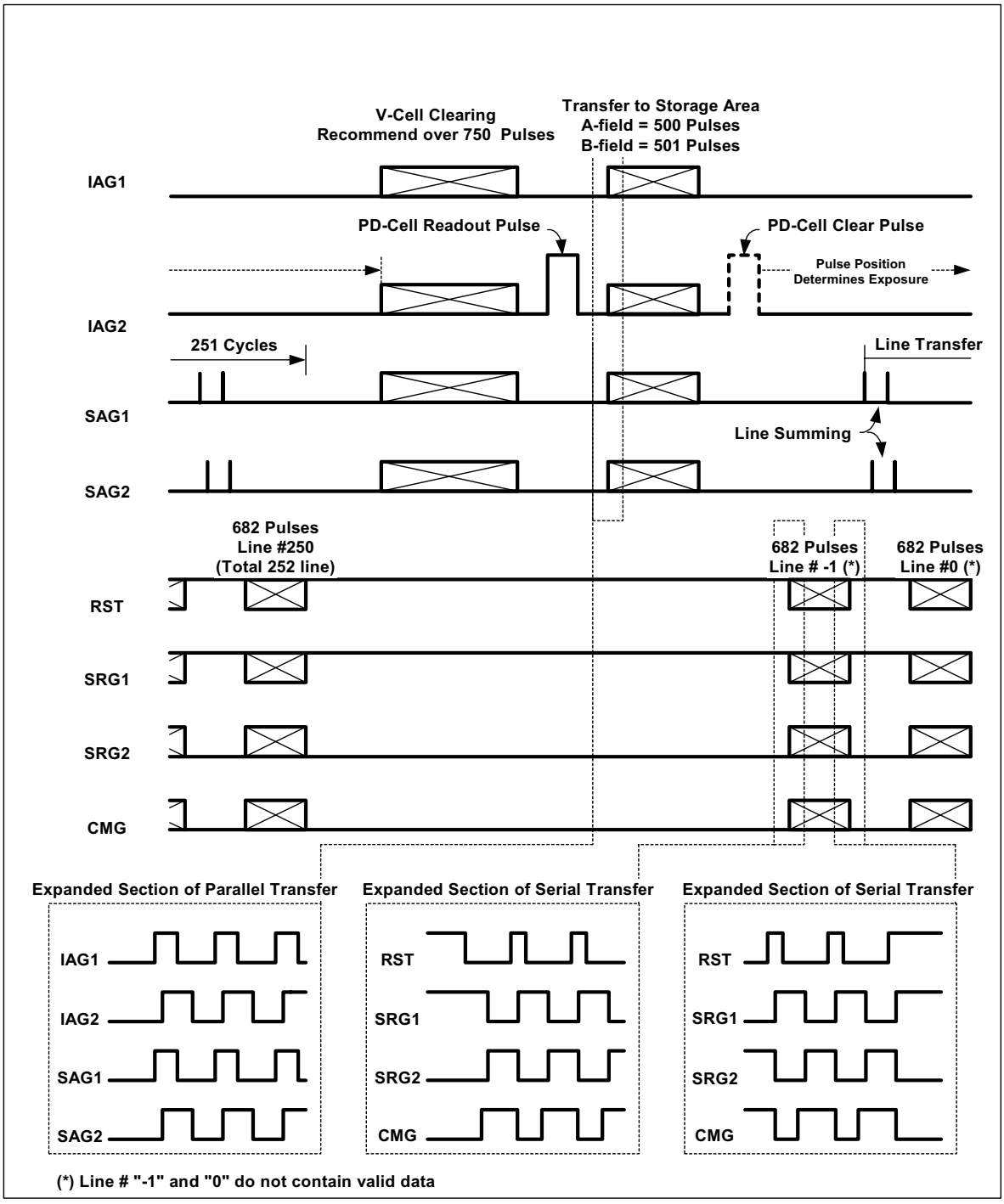


FIGURE 2-b. Interlace Timing of Line Summing Mode

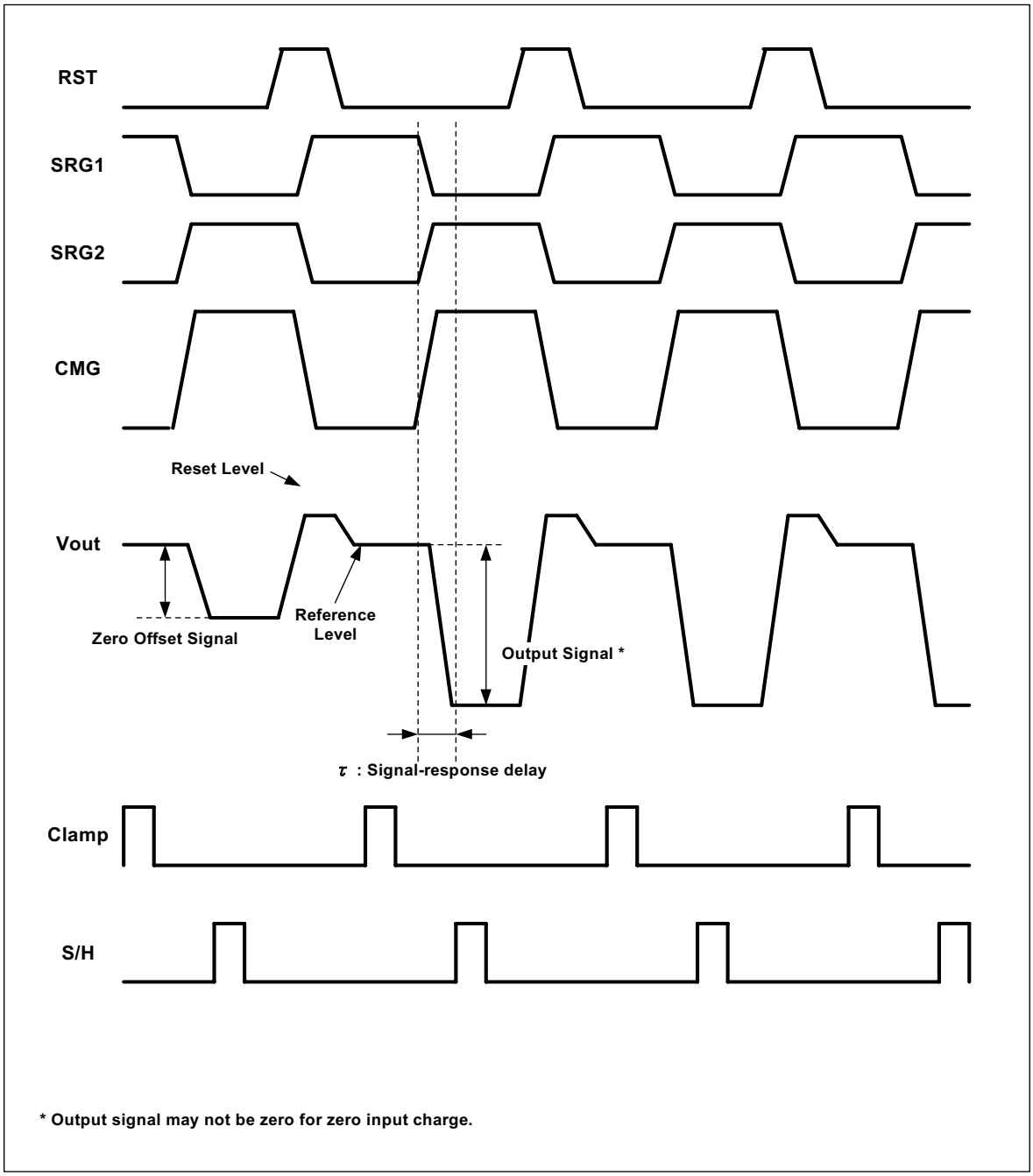
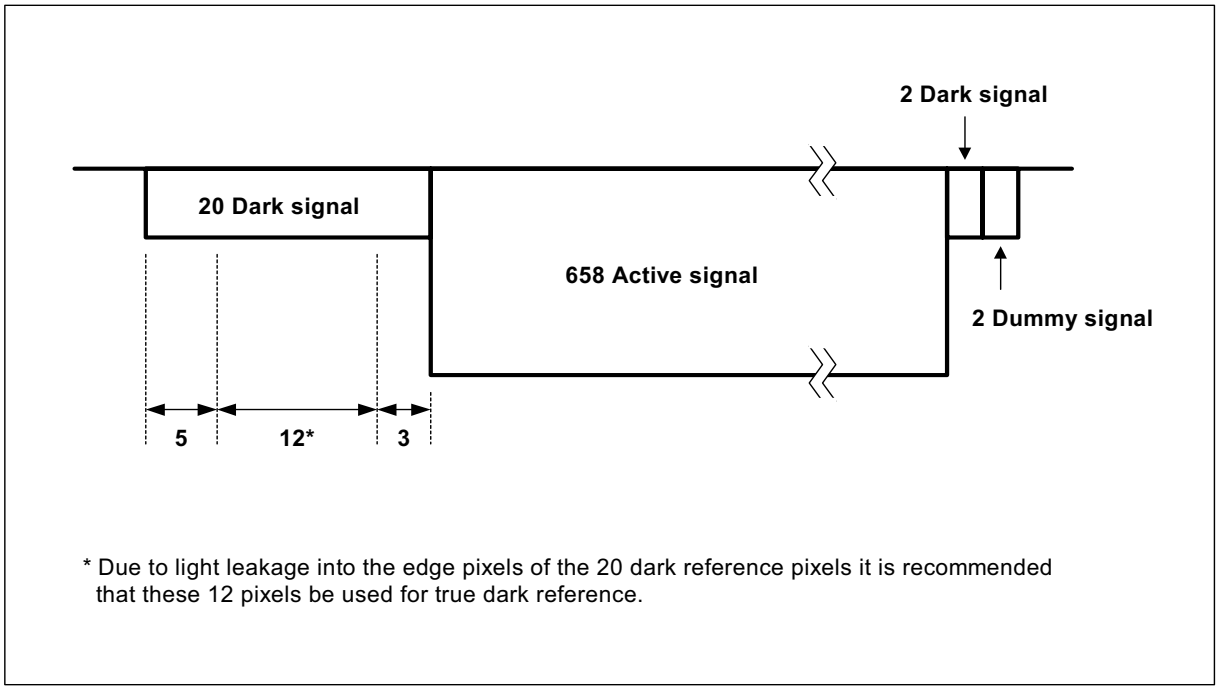
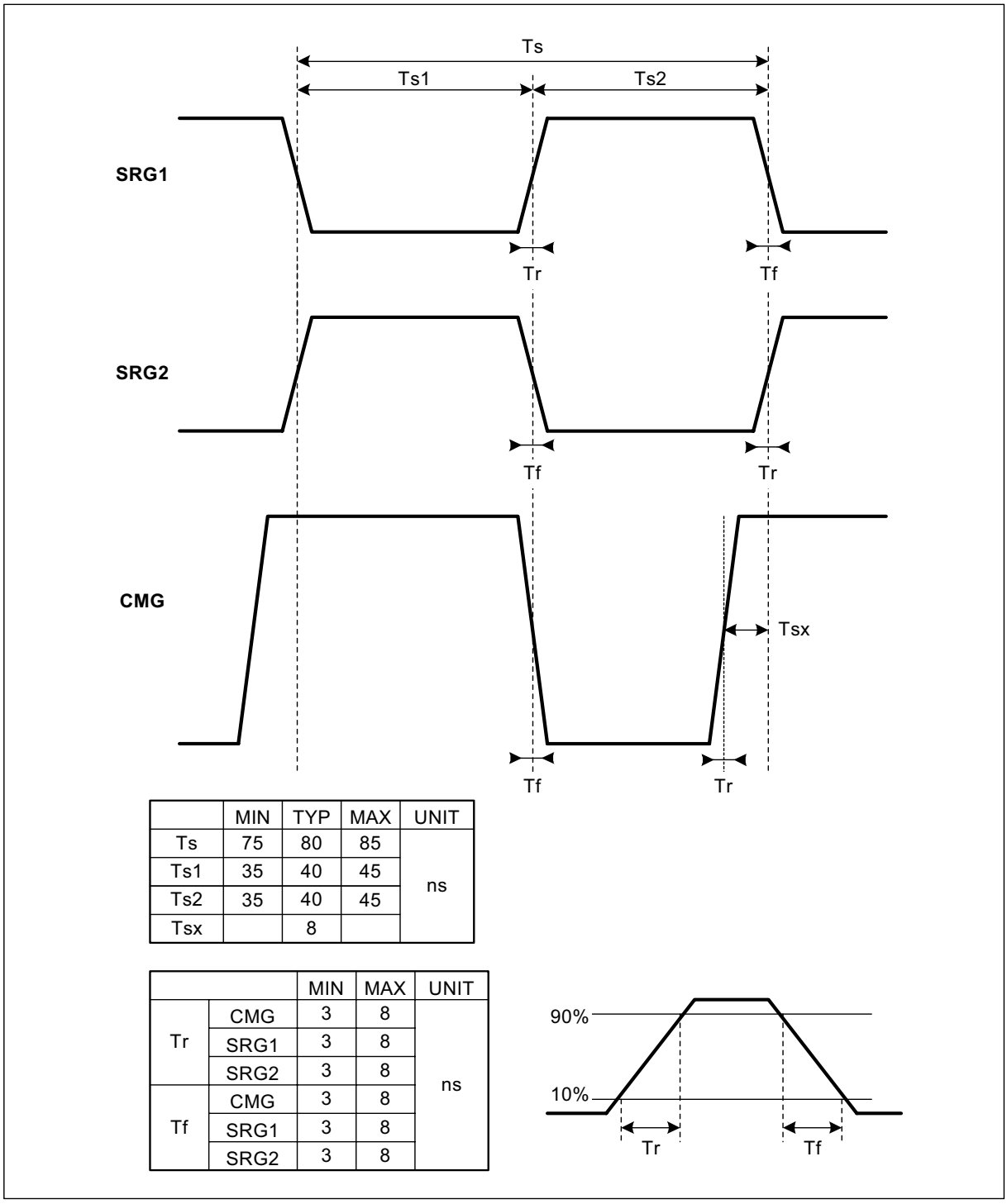


FIGURE 3. Serial register Clock Timing for CDS Implementation



* Due to light leakage into the edge pixels of the 20 dark reference pixels it is recommended that these 12 pixels be used for true dark reference.

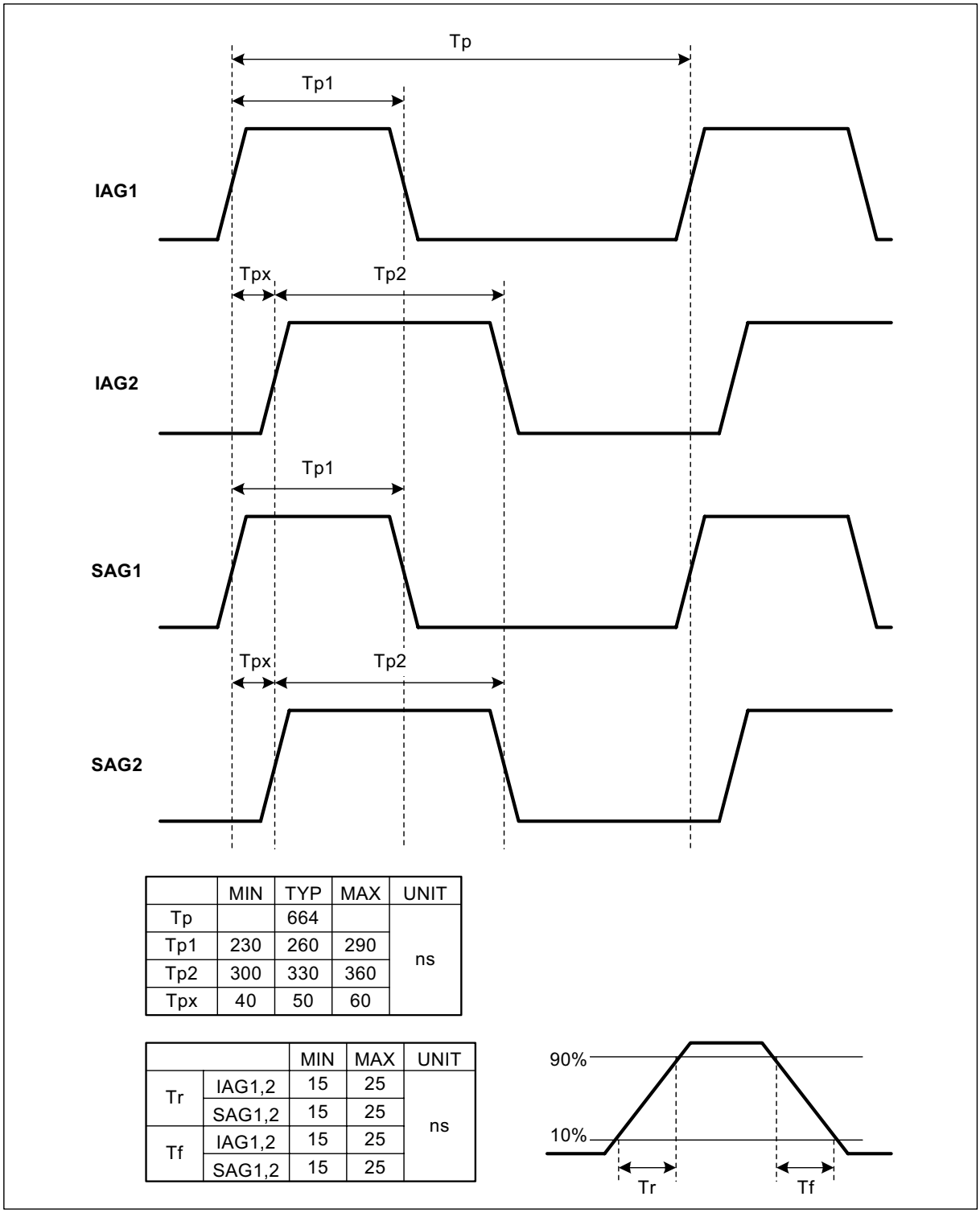
FIGURE 4. Detailed output signal



	MIN	TYP	MAX	UNIT
Ts	75	80	85	ns
Ts1	35	40	45	
Ts2	35	40	45	
Tsx		8		

		MIN	MAX	UNIT
Tr	CMG	3	8	ns
	SRG1	3	8	
	SRG2	3	8	
Tf	CMG	3	8	
	SRG1	3	8	
	SRG2	3	8	

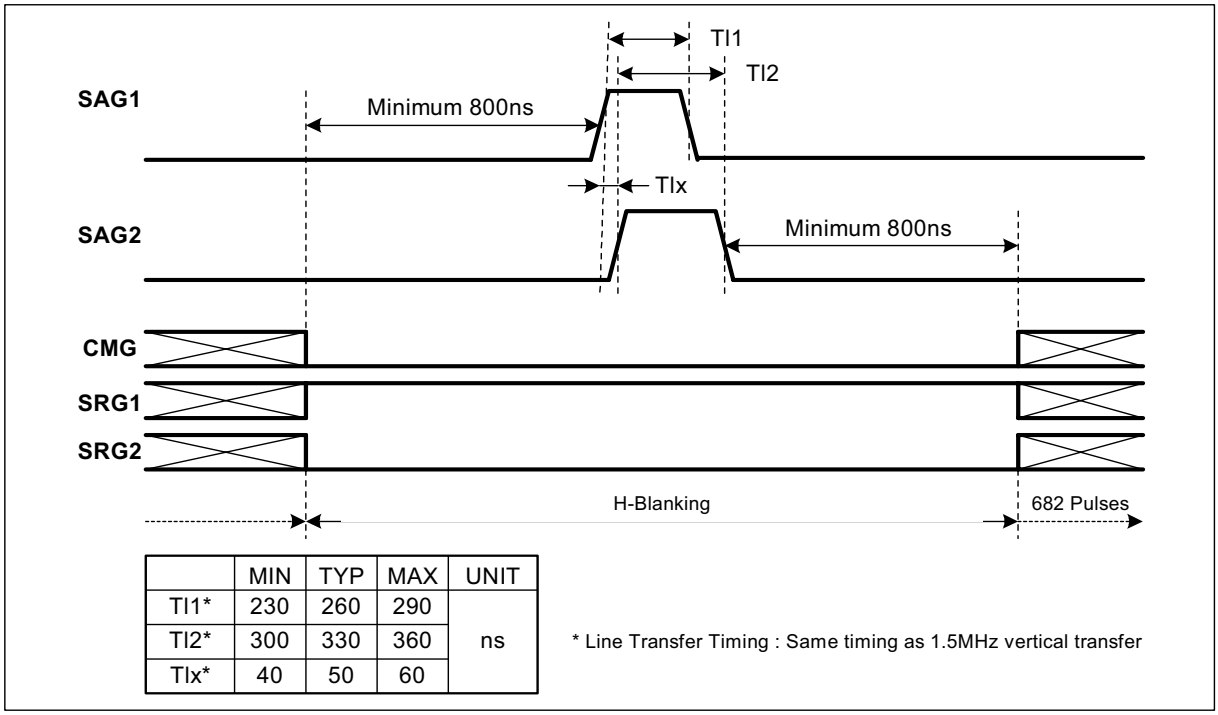
FIGURE 5. Serial Transfer Timing (12.5HMz applications)



	MIN	TYP	MAX	UNIT
Tp		664		ns
Tp1	230	260	290	
Tp2	300	330	360	
Tpx	40	50	60	

		MIN	MAX	UNIT
Tr	IAG1,2	15	25	ns
	SAG1,2	15	25	
Tf	IAG1,2	15	25	
	SAG1,2	15	25	

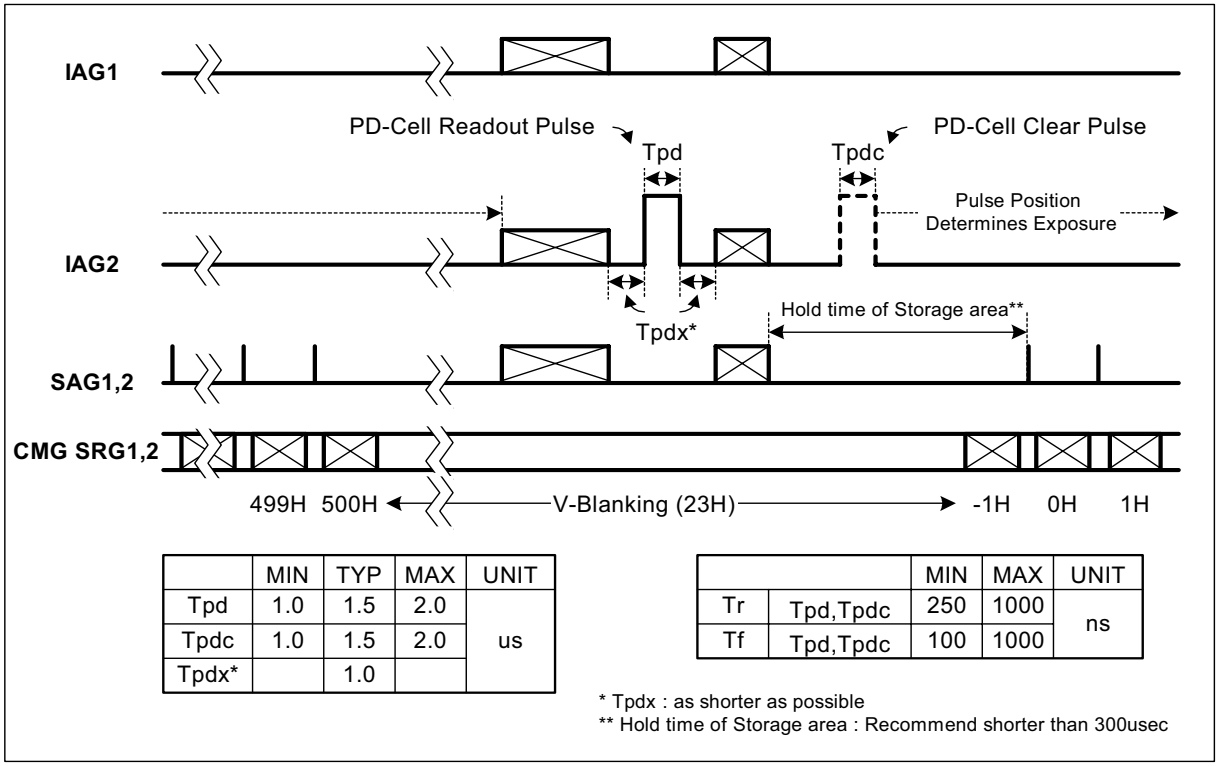
FIGURE 6. Vertical Transfer Timing (1.5 MHz application)



	MIN	TYP	MAX	UNIT
TI1*	230	260	290	ns
TI2*	300	330	360	
TIx*	40	50	60	

* Line Transfer Timing : Same timing as 1.5MHz vertical transfer

FIGURE 7. Typical Line Transfer Timing



	MIN	TYP	MAX	UNIT
Tpd	1.0	1.5	2.0	us
Tpdc	1.0	1.5	2.0	
Tpdx*		1.0		

		MIN	MAX	UNIT
Tr	Tpd,Tpdc	250	1000	ns
Tf	Tpd,Tpdc	100	1000	

* Tpdx : as shorter as possible
** Hold time of Storage area : Recommend shorter than 300usec

FIGURE 8. Typical PD-Readout and Exposure Control Timing

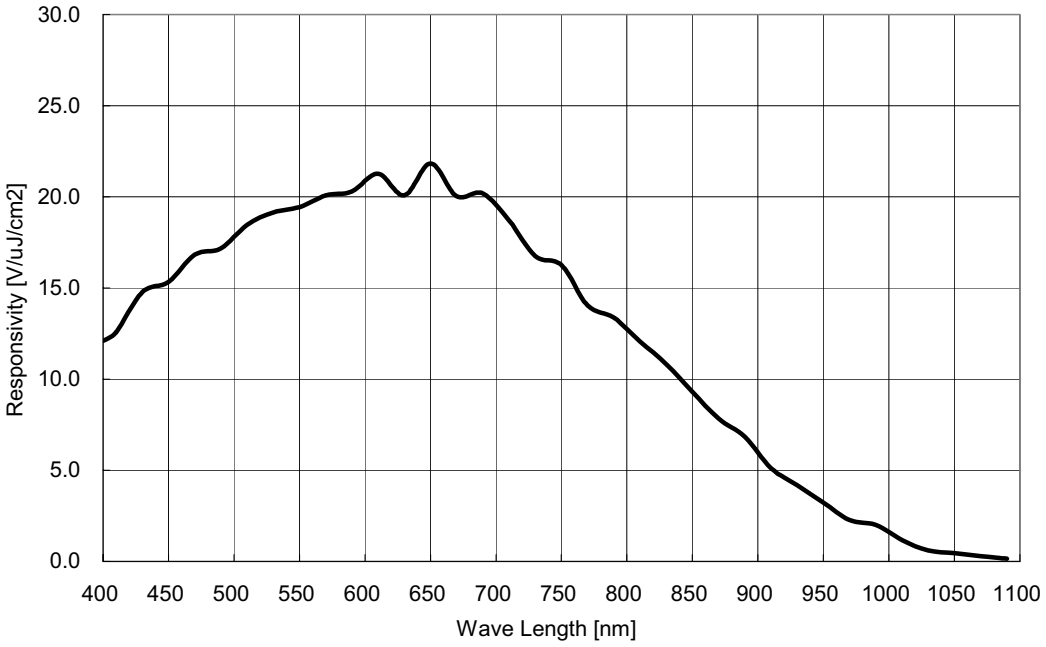


FIGURE 9. Typical Spectral Responsivity

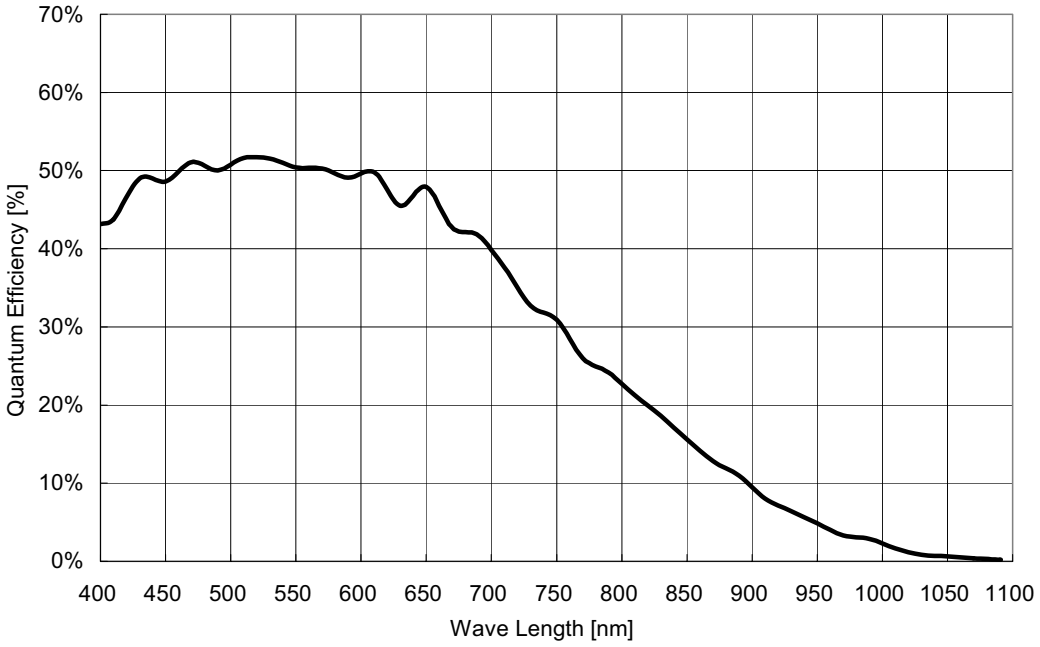


FIGURE 10. Typical Spectral Quantum Efficiency

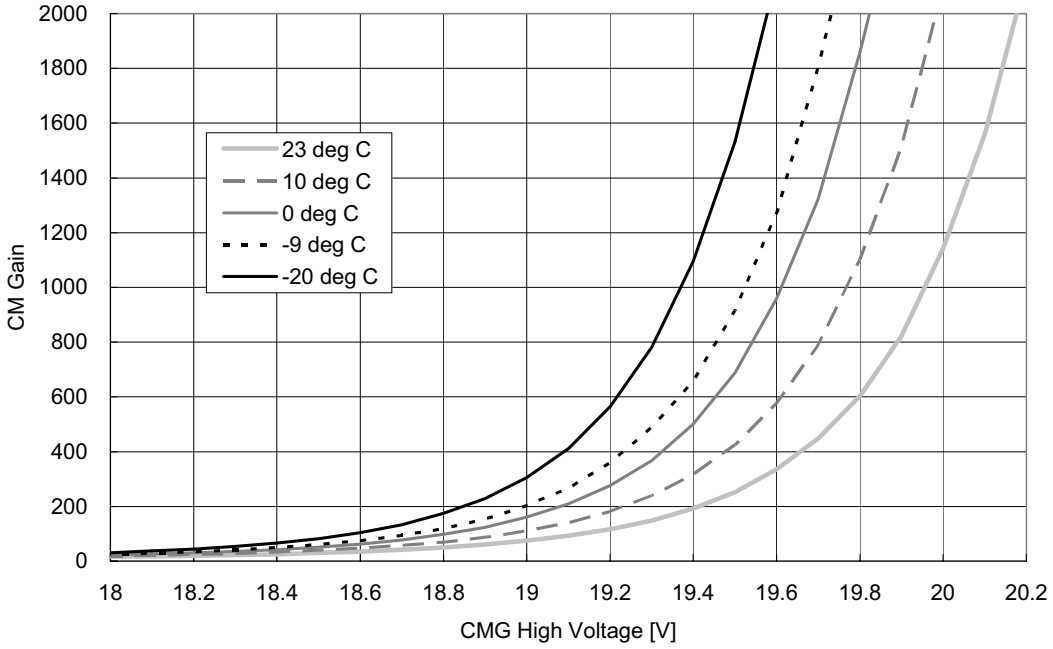


FIGURE 11. Typical Variation of Multiplication Gain with CMG High Voltage

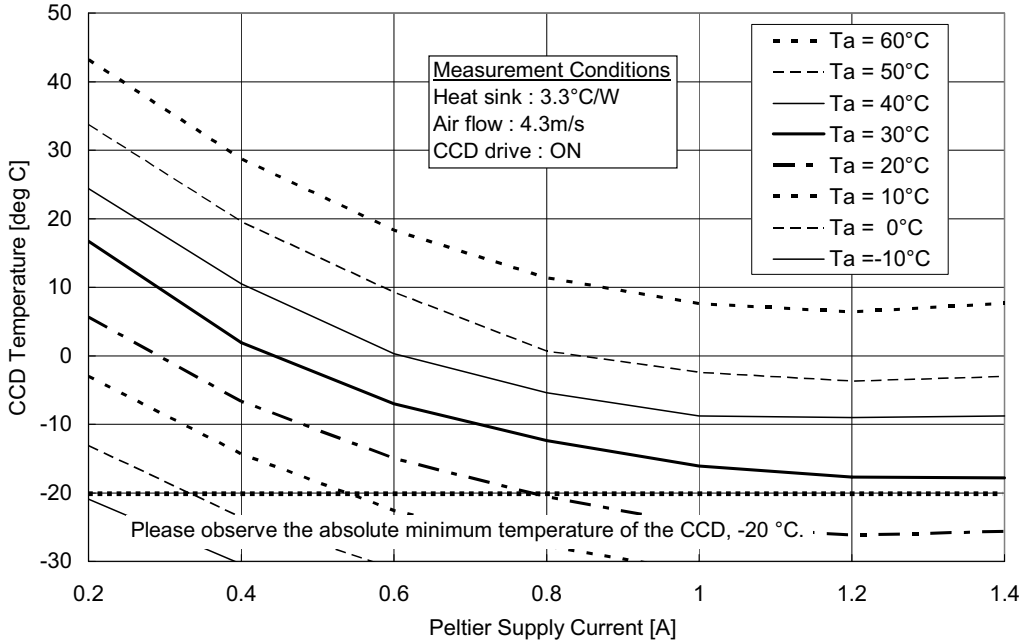


FIGURE 12. Typical Cooling Capability

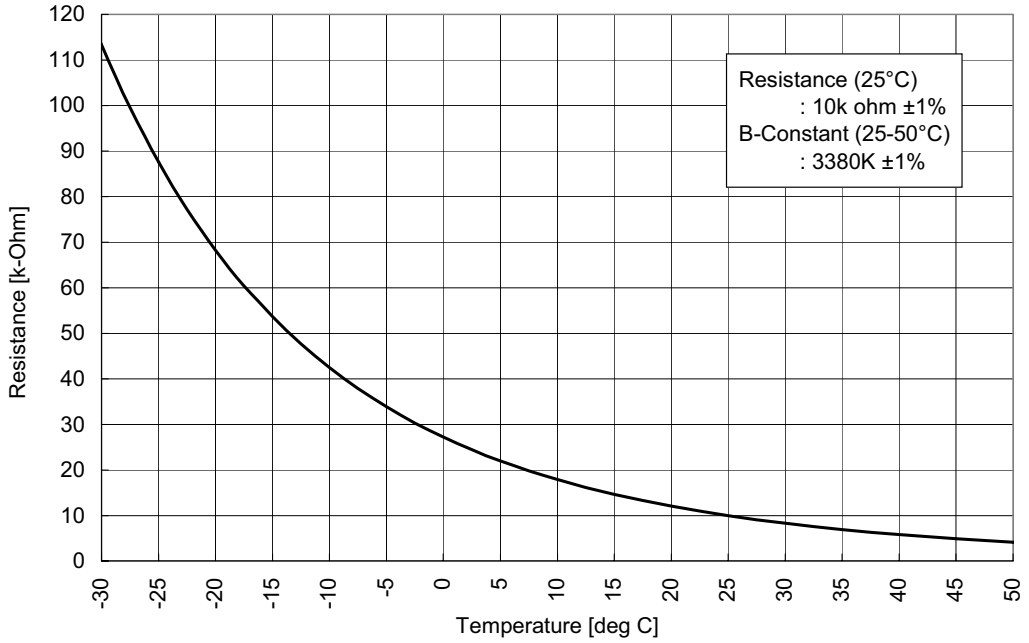


FIGURE 13. Typical Thermistor Characteristics

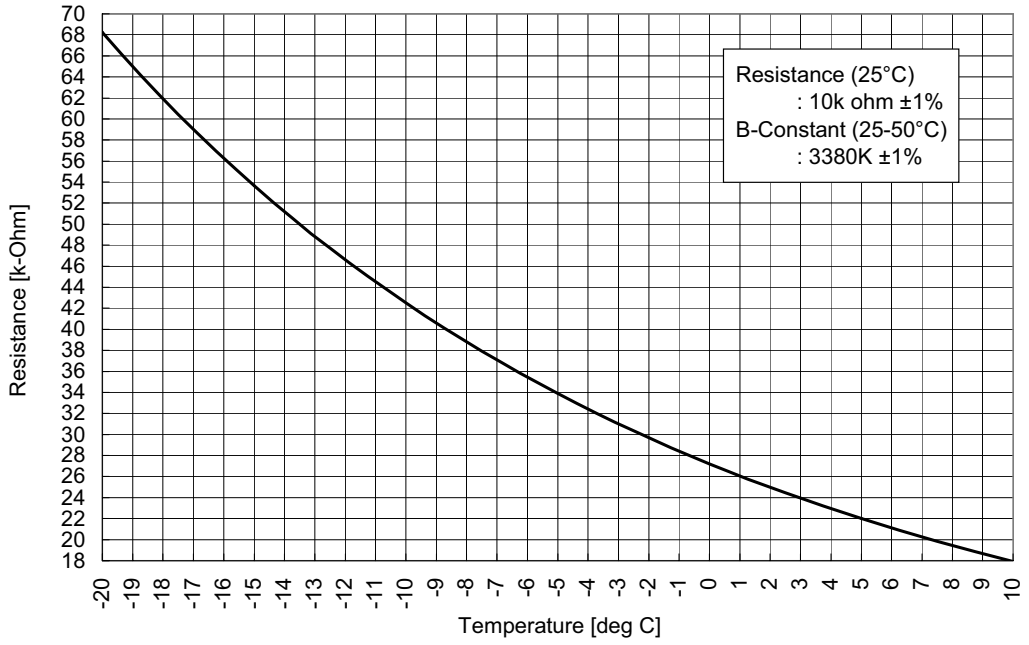


FIGURE 14. Typical Thermistor Characteristics (Detail)

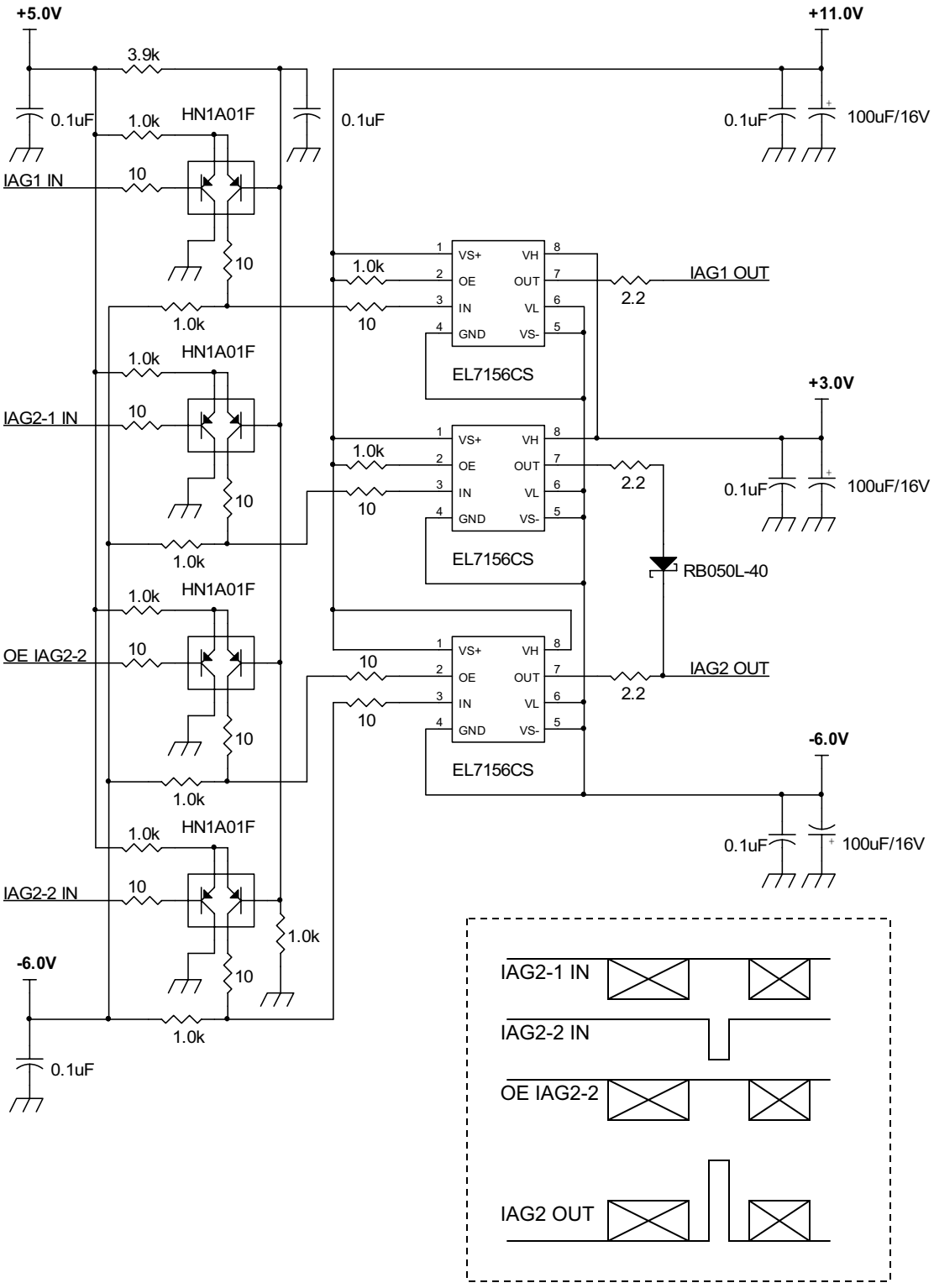


FIGURE 15. Typical IAG Driver Circuits

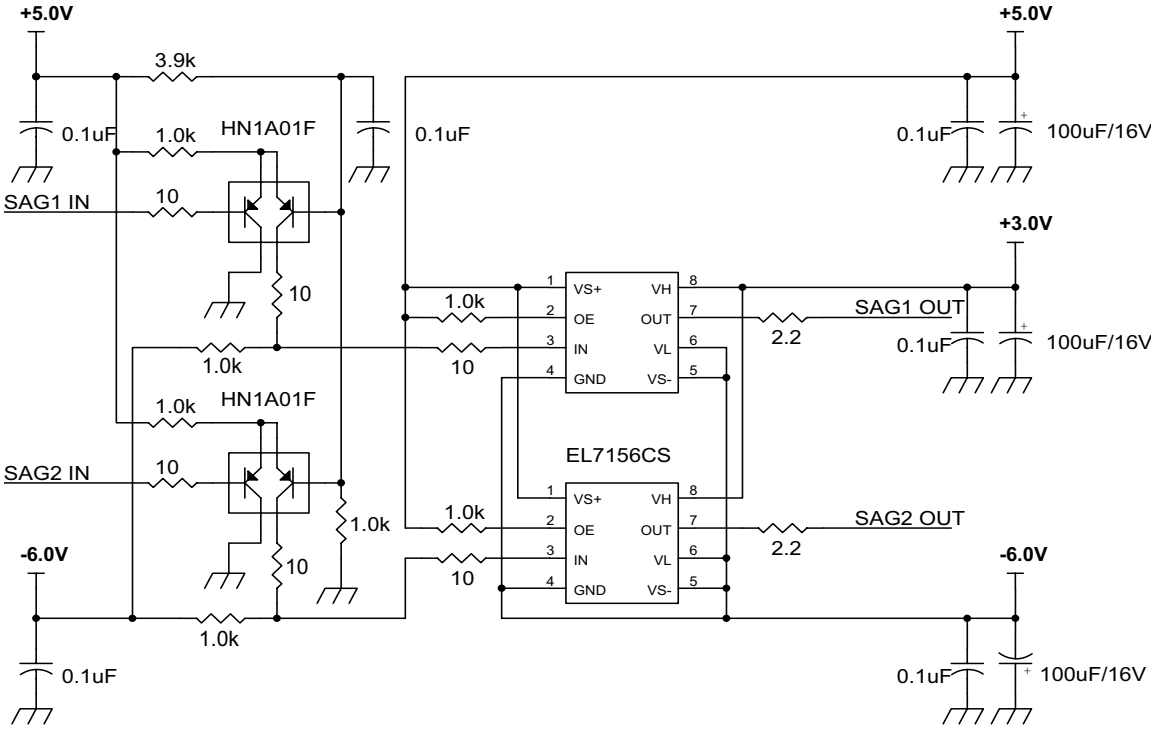


FIGURE 16. Typical SAG Driver Circuits

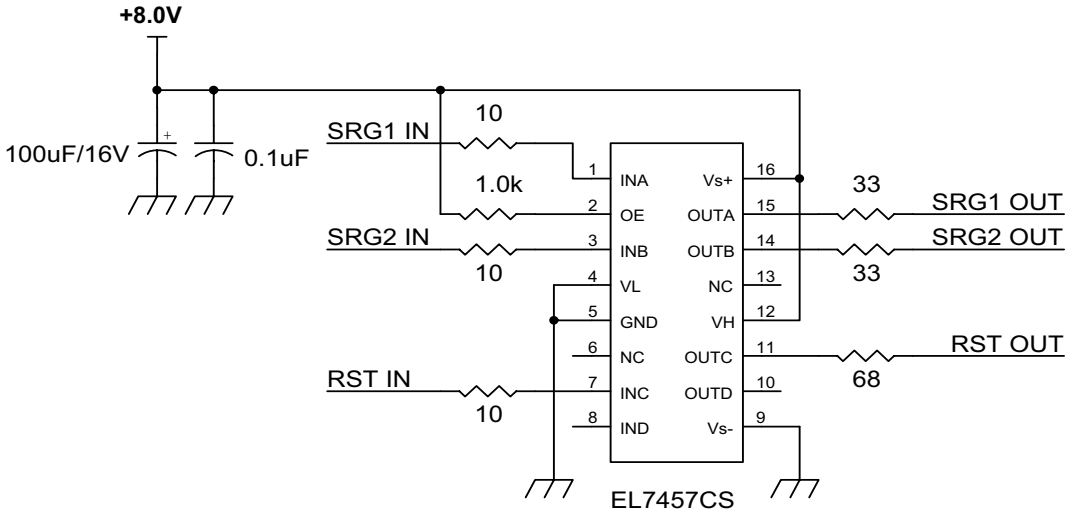


FIGURE 17. Typical SRG and RST Driver Circuits

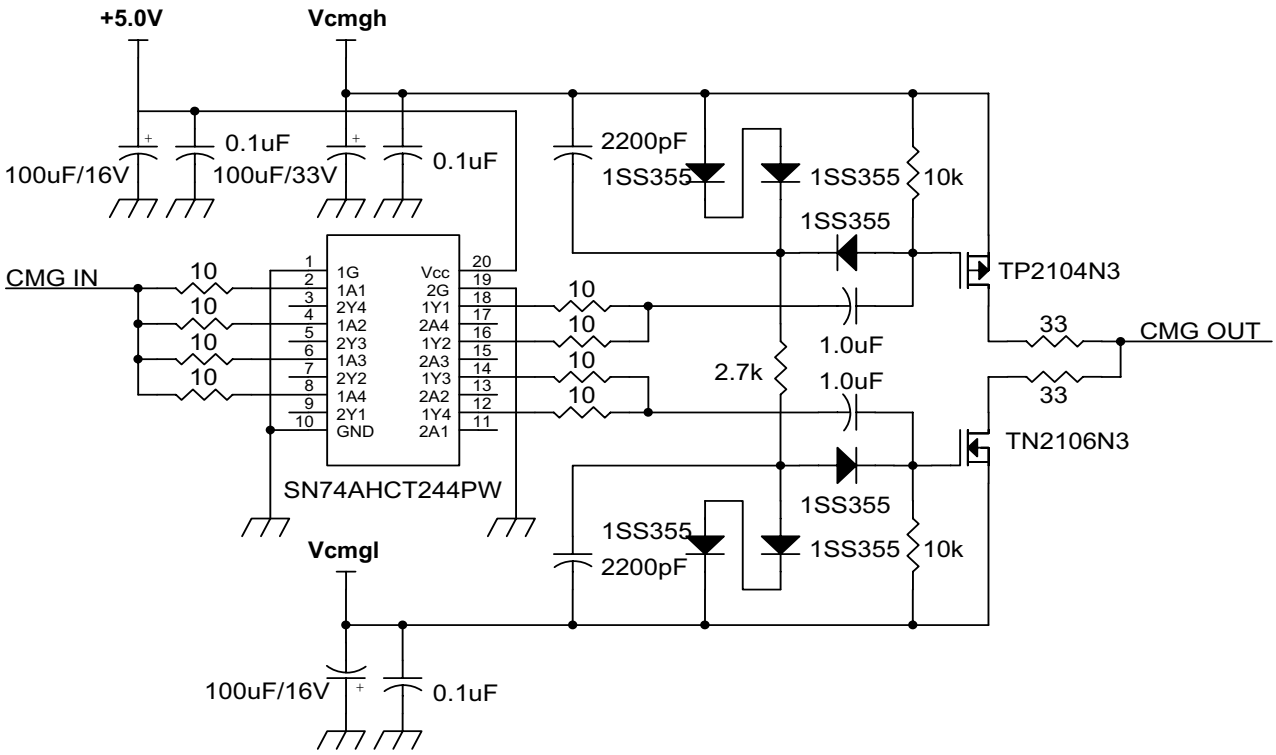


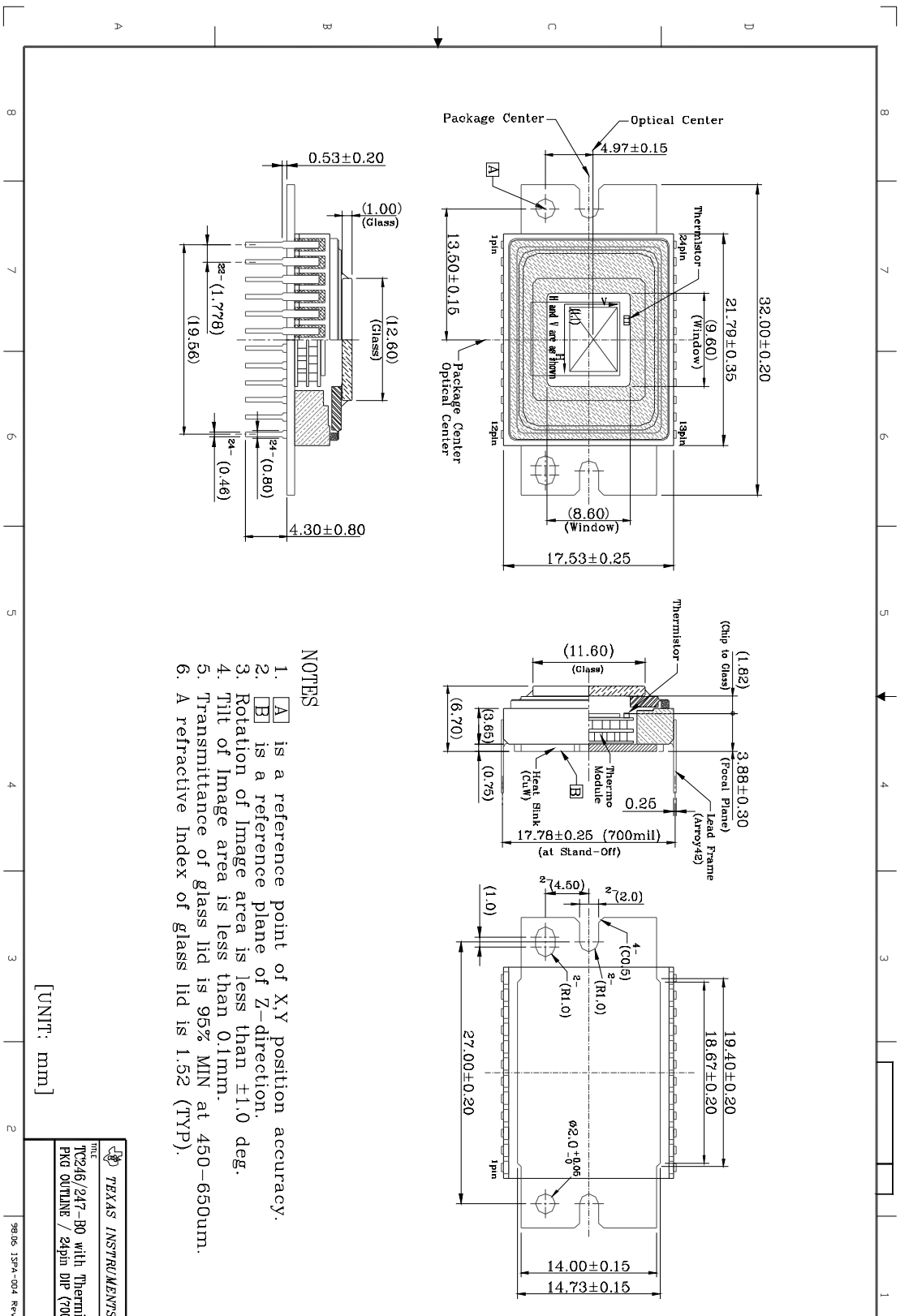
FIGURE 18. Typical CMG Driver Circuits

Mechanical data

The package for the TC247SPD consists of a ceramic base, a glass window, and a 24-pin lead frame. The glass window is hermetically sealed to the package. The package leads are configured in a dual-in-line arrangement and fit into mounting holes with 1,78 mm center-to-center spacing.

Attention

Be careful when attaching an external heat sink to the package. Fastening it too strongly may crack or puncture the package, making it susceptible to moisture or humidity.



NOTES

1. A is a reference point of X,Y position accuracy.
2. B is a reference plane of Z-direction.
3. Rotation of Image area is less than ±1.0 deg.
4. Tilt of Image area is less than 0.1mm.
5. Transmittance of glass lid is 95% MIN at 450-650um.
6. A refractive Index of glass lid is 1.52 (TYP).

[UNIT: mm]

TEXAS INSTRUMENTS
TC246/247-B0 with Thermistor
PKG OUTLINE / 24pin DIP (700mil)
98.06 13PA-004 Rev.03

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